Head Node

|  |  |  |  |
| --- | --- | --- | --- |
| Project (P15) | Current Rev 2 | 6/12/2022 | Jake Hafele |

HARdware Documentation

Jake Hafele

2022

|  |  |  |  |
| --- | --- | --- | --- |
| Revision History | | | |
| Rev # | **Description** | **Hardware Manager** | **Approved By**  **Need 2/3 for approval: eteam director or assistant director, eteam manager, or alumni** |
| 1 | **2021 ASC Rayce, reset for clarity** | **Si Yuan Sim** |  |
| 2 | **Added high side switches to control power relays, removed redundant charging logic, standardized power circuit with switching regulator** | **Jake Hafele** |  |

Contents

[**Theory of Operation** 3](#_Toc77106060)

[**Description** 3](#_Toc77106061)

[**Board Placement** 4](#_Toc77106062)

[**Purpose** 4](#_Toc77106063)

[**Application** 4](#_Toc77106064)

[**System Level** 4](#_Toc77106065)

[**Block Diagram** 4](#_Toc77106066)

[**Pin Diagram** 5](#_Toc77106067)

[**VDR Requirements** 6](#_Toc77106068)

[**Board Level** 7](#_Toc77106069)

[**Power Supplies** 7](#_Toc77106070)

[**Analog Fault Line** 7](#_Toc77106071)

[**External Kill** 8](#_Toc77106072)

[**Reverse Polarity and Fuse Blown Circuit** 9](#_Toc77106073)

[**Hardware Interface Logic** 9](#_Toc77106074)

[**Array Interface** 10](#_Toc77106075)

[**Relay Logic** 11](#_Toc77106076)

[**Current Sense** 13](#_Toc77106077)

[**Proof of Operation** 14](#_Toc77106078)

[**Test Procedure** 14](#_Toc77106079)

[**Test Results** 14](#_Toc77106080)

[**Troubleshooting** 14](#_Toc77106081)

[**Future Considerations** 14](#_Toc77106082)

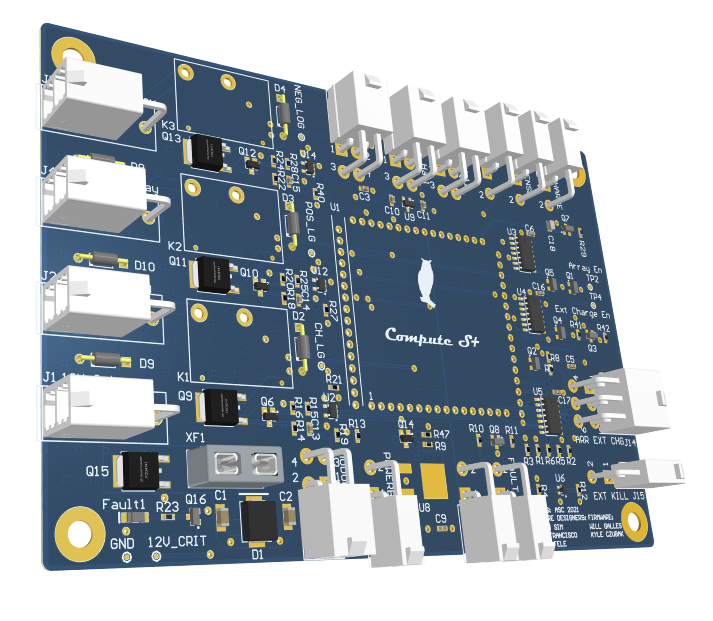
[**Additional Resources** 14](#_Toc77106083)

[**PrISUm Contacts** 14](#_Toc77106084)

[**Appendix** 14](#_Toc77106085)

[**Figures** 14](#_Toc77106086)

[**BOM List** 14](#_Toc77106087)



# **Theory of Operation**

## **Description**

Head node and module boards make up the Battery Protection System. Module boards gather data on pack operation and reports it back to head node. Using this data, array and pack interfaces are controlled. Most of the decision making and control is accomplished through the compute module on head node.

CAN is the primary digital communication protocol used in the car. The compute module CANH and CANL outputs are used for the main CAN bus. The pack network is looped through the modules and is terminated on one side at the end of the module board string. The other terminating resistor is located within Telem. This prevents the need for extra parts or different designs of module boards.

Module boards use a combination of software and hardware monitoring for voltage or temperature faults. The software monitoring and reporting is all handled using CAN as previously discussed. To get hardware fault information back to head node we have added an “Analog\_Fault” line connecting each module. This line is normally high and is pulled low by a temperature or voltage fault on any module. The logical state of this line is used for array and pack interface decisions.

Head node is also in charge of the isolation and connection of the pack to the rest of the system that powers the car. Hence, whenever the car is turned on into safe state, to drive or to charge, head node would be responsible for its operation. This is accomplished by having several relay logic circuitry that would turn on the three large relays located within the battery box that are responsible for positive terminal of the pack, negative terminal of the pack and a relay designated for charging. During the turn on sequence, head node also controls the operation of Powerboard which is signified through a digital signal that the battery pack is in a safe state enabling Powerboard to switch from child board to the Vicors to power the critical, main and party lines. During driving, head node also sends a signal enabling Precharge to turn on another larger relay that connects the pack to the motor controllers allowing the motors to be driven.

## **Board Placement**

Head board will be placed on top of Precharge. They will draw power from Powerboard’s 12V critical line.

## **Purpose**

Lithium-ion batteries are quite volatile and by competition regulations require complex management systems. PrISUm Solar Car chooses to design and build their own management system over an off the shelf unit.

# **Application**

## **System Level**

### **Block Diagram**

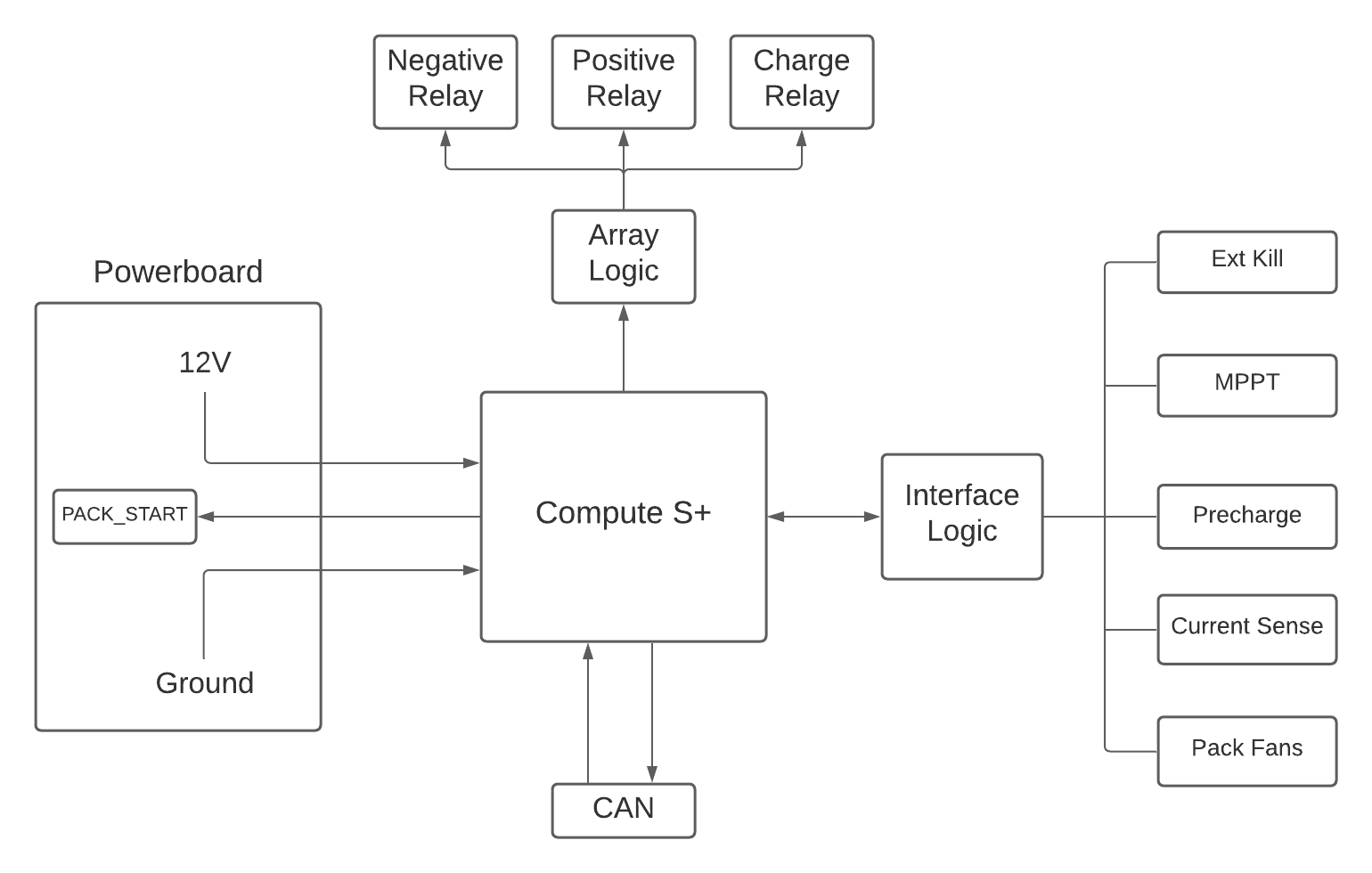
**

Figure 1 Block diagram

### **Pin Diagram**

|  |  |  |  |
| --- | --- | --- | --- |
| **Connector** | **Connector Type** | **Pin Number** | **Connector Function** |
| J1 | 2-Pin Megafit | 1 | Main Ground |
| 2 | 12V Critical from Powerboard |
| J2 | 2-Pin Minifit | 1 | Main Ground |
| 2 | Charge Relay Control |
| J4 | 2-Pin Minifit | 1 | Main Ground |
| 2 | Positive Relay Control |
| J5 | 2-Pin Minifit | 1 | Main Ground |
| 2 | Negative Relay Control |
| J3 | 4-Pin Minifit | 1,2 | Main Ground |
| 3 | 5V Analog Fault Line Start |
| 4 | 12V Critical to Module Board |
| J13 | 2-Pin Minifit | 1 | Main Ground |
| 2 | Analog Fault Line End |
| J7 | 4-Pin Minifit | 1 | 12V Critical |
| 2 | Main Ground |
| 3 | Pack Hall Effect Sensor Output |
| 4 | Main Ground |
| J9 | 4-Pin Minifit | 1 | 12V Critical |
| 2 | Main Ground |
| 3 | Array Hall Effect Sensor Output |
| 4 | Main Ground |
| J10 | 2-Pin Minifit | 1 | Precharge Drive Signal |
| 2 | Main Ground |
| J11 | 2-Pin Minifit | 1 | Powerboard Current Sense |
| 2 | Main Ground |
| J17 | 2-Pin Minifit | 1 | Powerboard Pack Start Signal |
| 2 | Main Ground |
| J15 | 2-Pin Minifit | 1 | External Kill Switch |
| 2 | Main Ground |
| J6, J8 | 2-Pin Minifit | 1 | CAN High |
| 2 | CAN Low |
| J12 | 4-Pin Minifit | 1,4 | Main Ground |
| 2 | 12V Critical |
| 3 | Fan Control |
| J14 | 6-Pin Minifit | 1 | Array Switch |
| 2 | External Charge Switch |
| 3 | Array Relay |
| 4 | Main Ground |
| 5 | Open |
| 6 | Open |

### 

### **VDR Requirements**

5.2.E.3 – *Over Temperature Set Points*

|  |  |  |
| --- | --- | --- |
| **Battery State** | **Low(˚C)** | **High(˚C)** |
| Charge | 10˚C | 45 ˚C |
| Discharge | -20 ˚C | \*60 ˚C |

*\*Monitored by hardware. All others in software*

5.2.E.4, 5.2.E.5 – *Under and Over Voltage Set Points*

*Battery Module Voltage Warnings and Limits*

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Trip Point (Volts)** | **Hardware Monitored** | **Software Monitored** |
| Voltage Low Warning | 3.0V |  | x |
| Voltage Low Fault | 2.8V | X | x |
| Voltage High Warning | 4.0V |  | x |
| Voltage High Fault | 4.2V | X | x |

5.2.E.6 – *Over Current Set Points*

*Pack Current Limits for Charge and Discharge*

|  |  |
| --- | --- |
| **Battery State** | **Current Limit** |
| Charge | 40.0A |
| Discharge | -50.0A |

5.2.E.8 – *Start-up and Fault Handling*

When the start process for the car has been initiated by flipping the main switch. The Auxiliary Line will power BPS and critical systems. At this point Head Node will begin polling each individual module through CAN, checking for continuity, voltage measurements and temperature measurements for any faults. If all modules report OK, then the start-up process continues by allowing our Precharge and Powerboard systems to provide power to the rest of the car and close the relays connecting the main pack to the rest of the electrical systems within the car.

The job of every Module Board is to record and report data back to Head Node. When a fault occurs in a battery module, it will be reported by hardware back to a digital kill circuit on Head Node which will open the relays. It will also be recorded by software and reported over the CAN bus to active the BPS strobe and driver fault indicator.

5.2.E.9 – *Static Firmware*

In order to comply with Regulation 8.4F BPS software must be unmodified after scrutineering and tamper proofing must be implemented. Head node has header pins used to program the microcontroller using JTAG standards. These pins will be covered in taper proof tape and signed by the scrutineer. This will prevent the modification of software on any head node.

5.2.E.10 – *Driver Dash and BPS Strobe*

The fault CAN message reported by BPS will be picked up by Rear Hal and activate the BPS Strobe. The same message will also be picked up by the driver display and indicates to the driver a BPS fault occurred. When the relays are open HAL, BPS, and Driver Dash are powered by an auxiliary pack.

## **Board Level**

### **Power Supplies**

Power for Head node and module boards is supplied by 12V\_Crit from Powerboard. This is regulated down to 5V using a R-78AA5.0-1.0SMD-R switching regulator. It should be noted that in Rev 2 of this board, we standardized the regulator to the same switching regulator that is used on the application boards like buttonboard or motorboard. Previously, the regulator was a linear regulator. The regulator is 1A capable, but Head Node only requires ~30mA to operate in normal conditions.

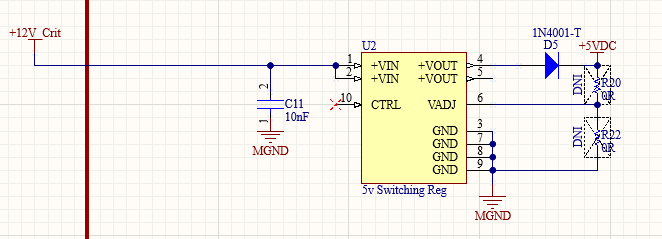
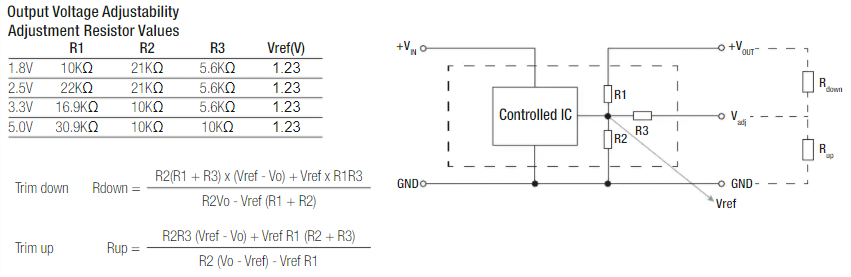


Figure 2 5V Linear regulator circuit

Due to the diode D5, there is a voltage drop around 0.6V from the output of the switching regulator. The diode is recommended in the datasheet to be included for protection of the regulator and output. By default, the trim up and trim down resistor are left open in the circuit. To adjust the output voltage higher, we can find a value for the trim up resistor so that after the voltage drop of the diode it will output 5V. According to figure 5, if we include a diode before VOut we need to add that voltage drop onto **Vo**, which will be roughly 0.6V. After plugging in values of **R1**, **R2**, **R3**, **Vo**, and **VRef** for the values spec’d out at the 5V switching regulator, we get a trim up resistor of 47 kOhms. Based on the protection diagram in Figure 5, we **do not** need to include a trim down resistor, and only a trim up resistor.

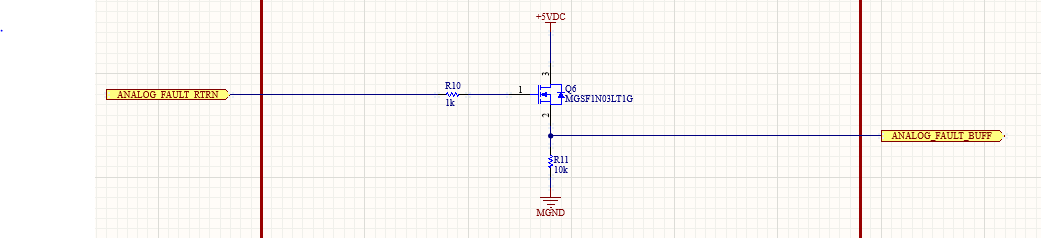


There used to also be a 2.5V regulator to be used as a reference, but was removed as it was unused in previous revs of the board.

### **Analog Fault Line**

The analog fault line is provided by head node to the first module board in the chain. It is a 5V signal and a jumper resistor was previously included for testing and removed due to consistency in performance.

To receive the analog fault line from the 35th module board, which is the module board at the very end, a buffer circuit is required. This is because the line from the back of the network is very long and there might be considerable losses resulting in a very weak signal. Hence, a n-channel MOSFET was used to buffer it. When the analog fault return line is high, it drives the diode between the gate and source turning the MOSFET on. Conversely, it would turn off when the analog fault line goes low. This signal is fed to the MCU as well as the logic interface hardware. This gives us both hardware and software redundancies making the system even safer. This line used to be driven with a BJT, but was removed due to scarcity of BJT’s in our electrical system and easier part availability of 5V MOSFETs.



### **External Kill**

According to regulations, the car must possess an external kill switch that can be accessed from the outside of the car. This switch should allow for any person to immediately shut down the system and isolate the battery pack in case of an emergency. The switch is connected to a 2-pin minifit connector, and it is typically **closed** in a normal state. This would pull the uC\_EXT\_KILL node **low** giving it a digital signal of 0. To shut down the car immediately, the switch would need to be flipped to the **open** state causing the node to be **pulled up to 5V** through a 10kΩ resistor. This was done with the fact in mind that the connectors coming loose would also act as an open switch pulling the node up. It would prevent us from driving without any knowledge that the external kill switch is no longer working.

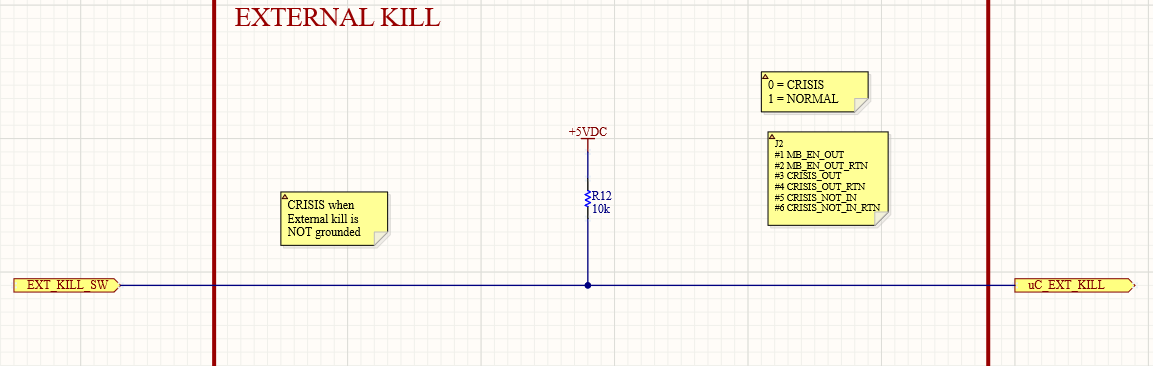


Figure 5 External kill

### **Reverse Polarity and Fuse Blown Circuit**

To protect the board from human error if a connector were to be plugged in reverse, a reverse polarity diode is used. This requires a simple P-channel MOSFET where the gate is connected to ground and the source and drain acting as the typical conducting path. In a normal case where the connector is plugged in correctly, the gate would be ground at 0V, and the source would be at 12V. This would have a gate-to-source voltage of -12V turning the MOSFET on thereby powering the entire board. However, if it were to be reversed, the gate-to-source voltage would instead be 12V which would disable the component preventing any other part in the circuit to be destroyed.

The fuse would protect the board from any excessive current draw, and it is set to less than 5A currently due to the current draw from the large relays in the battery box. This might not prevent any components from being destroyed however it would stop it from burning or blowing up as it would cut off the supply. Once again, a P-Fet is used as a good fuse would conduct the 12V to the gate causing the gate-to-source voltage to be 0V turning it off. However, burning the fuse would mean a -12V gate-to-source voltage which would cause the P-Fet to conduct and draw current into a resistor through the 12V supply and current limited by a 1kΩ resistor.

A TVS diode is also used for any high voltage transient suppression (ESD). However, a Zener diode should also be looked into in the future as a clamping mechanism as ESD is typically not as much of a concern for many of our purposes whereas over-voltages happen a lot more regularly within this team.

The ferrite bead FB1 and the capacitors C1, C2, C9, and C13 are all used to smooth out the 12V Critical signal coming from powerboard. This was added in Rev 2 of this board as a standardization for each board that has the same power circuit. The capacitors have decreasing amounts of capacitance to help keep a constant 12V supply for the 5V switching regulator and 12V Critical parts.

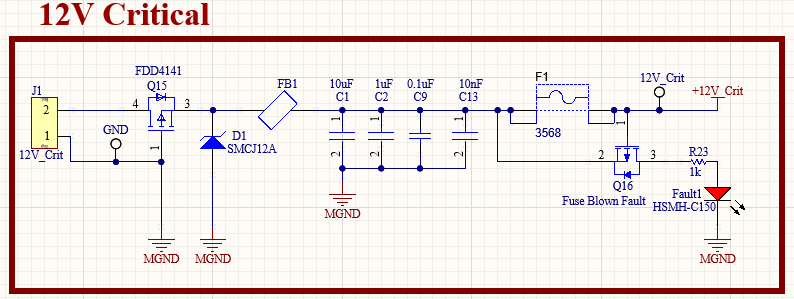


Figure 6 Reverse protection and fuse blown circuit

### **Hardware Interface Logic**

The logic that controls much of the operation of head node is located in this circuit. Three AND gates within the same package are used that controls three aspects that are: turning on the car, enabling array charging and enabling external charging. However, external charging has a different implementation, and the current circuit is a leftover remnant from Penumbra’s head node. This includes both circuits in Figure 7 and Figure 8.

For the turn-on operation, three signals are required to turn on the AND gate which produces a high signal (START\_EN) that propagates to the three logic circuits that would control the operation of the three large relays within the battery box for positive terminal, negative terminal and external charging. The three signals required are:

1. ANALOG\_FAULT\_BUFFER – Analog fault line
2. uC\_Fault\_F – Software controlled fault signal
3. uC\_EXT\_KILL – External kill switch which defaults to 0 as “good” which is why an inverter is used to turn on the AND gate.

Similar to the battery pack turn on logic, three signals are also needed for array logic, one software fault signal, one hardware and one software switch enable lines for redundancies. They are specifically:

1. uC\_Fault\_F – Software controlled fault signal
2. ARRAY\_EN – Software controlled array enable signal
3. ARRAY\_SW – Hardware controlled array enable signal

The output of this AND gate signal for arrays would then be XORed with the same exact logic circuit for external circuit (not in use). This means that if the ARRAY\_TRIGGER signal were to be high, array charging will always be enabled since this external charge logic is disabled. Hence, in order to ensure that both external charge and arrays are not enabled at the same time (since external charge is controlled in a separate logic), software has to be written in order to ensure that only one of the functions are on at the same time.

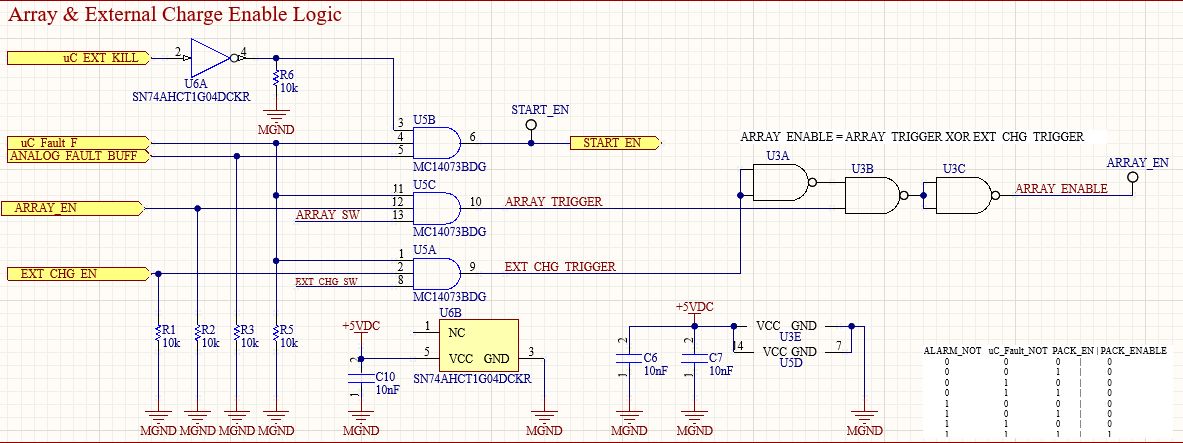


Figure 7 Hardware interface logic

### **Array Interface**

As mentioned earlier, the external charging interface here is outdated but is still in use for arrays. The two MOS circuits on the left are the switch circuits that lead to the AND gate logic earlier. N-channel MOSFETs are used since if the switch were closed and connected to ground, that would mean the device is turned off and connected to ground propagating a high signal. Conversely, if the switch were to be opened, the gate is connected up to 5V turning the device on and connecting the ARRAY\_SW node to ground. This has similar intent to the external kill logic since a disconnecting connector would not artificially induce a high signal but instead kill the entire charging operation which would alert users appropriately.

The circuit on the right side on the figure instead is used to control a signal that is sent out of the board after the computed logic and to its respective destination of array relay board. After fulfilling all the conditions necessary, the N-channel MOSFETs are turned on causing them to propagate a low signal.

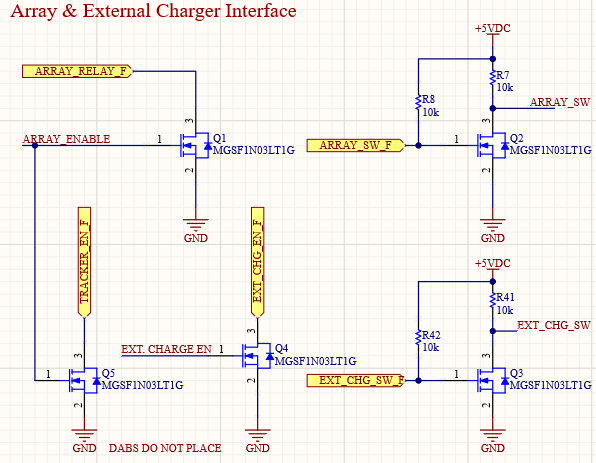


Figure 8 Array and external charge interface

### **Relay Logic**

The large relays within the battery box that are not installed on any battery box are driven by the control relay logic housed on head node. There are two stages that control its operation. The first stage is a two input AND gate that turns on either a relay or a power switch that is used to drive the larger off board relays (Figure 9).

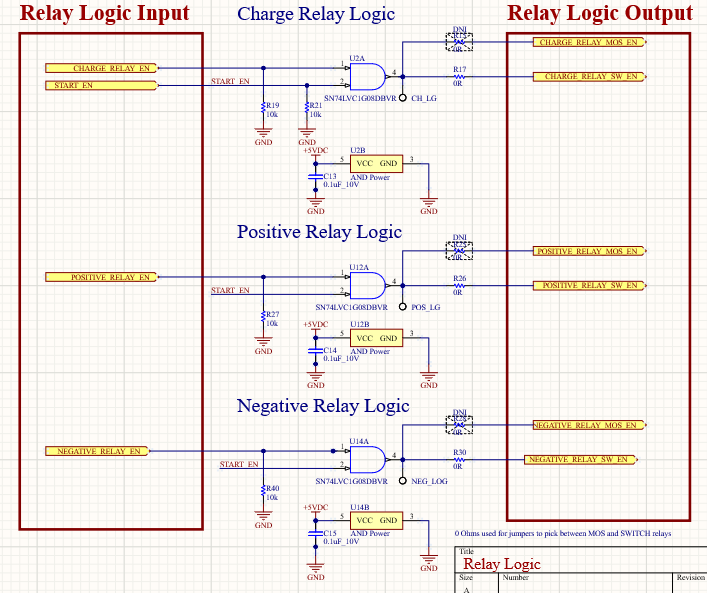


Figure 9 Control logic to turn on onboard relays

### **Power Switches**

The power switches use the relay enable output from the above logic to power the external relays for the positive, negative, and charge relays. The power switches are very simple according to its datasheet with no decoupling necessary and only a 10kΩ current limiting resistor was required to turn on at the enable line. This would protect the MCU during overvoltage and during reverse battery condition. The current sense was also going to be ignored on this board since there is a limit on the number of analog input pins and there is no big need to measure these currents. But the resistor values used were suggested by the manufacturer. The output current is determined the sense resistor which is 1kΩ with the 10kΩ resistor being used for protection. The current sense output would be a current which is determined using the equation below.

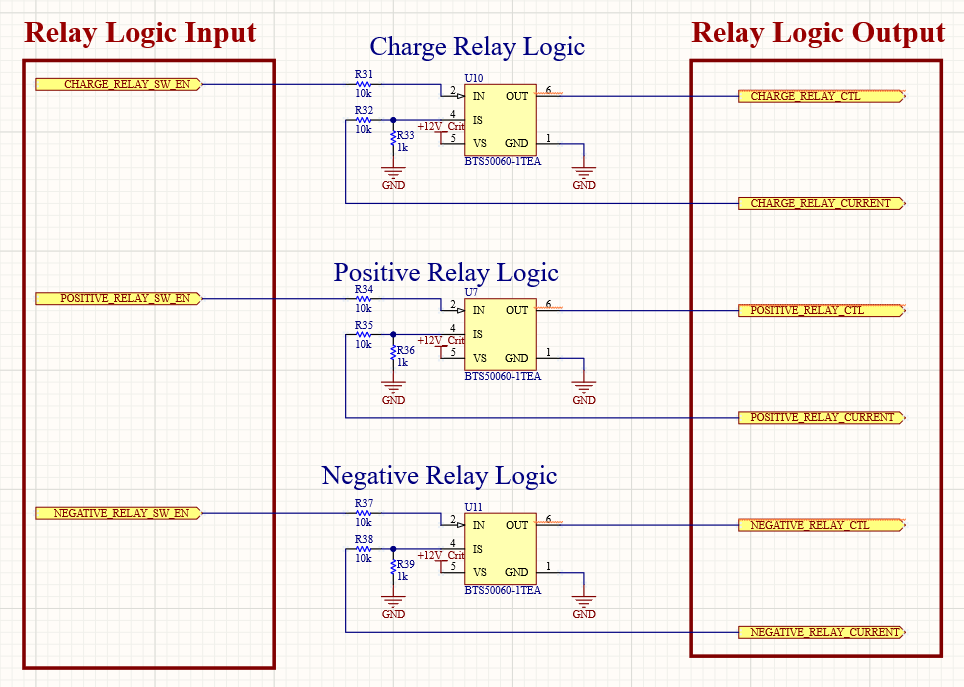


Figure 13 Power switches to turn on large off board relays

### **Current Sense**

Another aspect of head node is sensing the current that is flowing from the arrays into the pack as well as the current that is being used by the motor controllers to power the motors. To achieve this, hall effect sensors from Honeywell are used, CSLA2DG. These sensors can sense both AC and DC current which is ideal since regen would also send power back to the pack which would be useful information to obtain. They also run on 12V Critical supplied by head node and output 6V at 0A nominally. However, it was found that there are quite large differences between different components, and they need to be characterized in order to have an accurate read.

The characterization process includes looping a wire around the hall effect sensor multiple times in order to artificially generate a larger magnetic field which we can translate into a large current. This is because the bench power supplies can only generally reach up to 5A and it is an easy way to know the current flowing through the wire. Through testing, it was found that a looping a wire around just once would double the “current” compared to a straight wire just going through the middle of the hall effect. Hence the equation to generalize the current would be:

The characterization for one of the hall effect sensor used can be found in Figure 11 and it can be seen that it is extremely linear. But the downside of this hall effect sensor is that its maximum current sense is at 150A which is double our maximum expected output at 80A. This means that we would be unable to full advantage of the resolution of the ADC on the MCU on S+. This was caused by a lack of supply for the other models. Another note is that there is a need to subdivide down the output voltage from 12V (max) to 5V (MCU voltage) to prevent burning an S+. This was accomplished by a simple voltage divider with a ratio of 5/12.

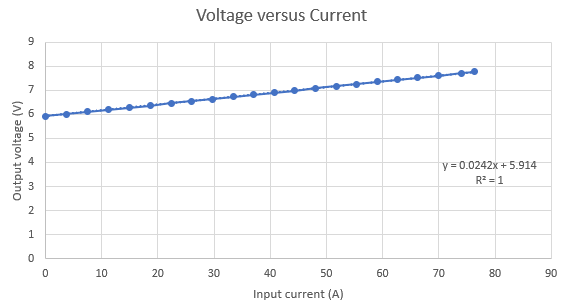


Figure 11 Linear regression model of hall effect sensor

### **Precharge and Powerboard Interface**

Precharge and powerboard propagate a signal from the MCU on compute which is then buffered using the same circuit. Powerboard requires a 12V signal hence the same circuit used on the previous relay buffer is also used here and it operates the same. The precharge buffer on the other hand uses a BJT in a common collector configuration. A high signal drives the body diode of the BJT between the base and emitter turning the component on drawing current from the collector to the emitter which would drive the signal across a wire to precharge which is located below head node.

Precharge and powerboard propagate a signal from the MCU on compute which is then buffered using the same circuit. Previously, a 12V signal was buffered with two mosfets for powerboard from a 5V signal, but this buffer has now been updated and moved to powerboard and a 5V signal is now buffered to powerboard. Now, the buffer is done with a p-channel MOSFET. When the powerboard enable signal is 0V, or “enabled”, current will conduct between the gate and source and in turn conduct 5V to the outputted powerboard signal. With 5V applied, the MOSFET will turn off and powerboard will apply 0V through the MGND connected to the resistor by the drain of the MOSFET. It should be noted that the software logic has changed on headnode, as previously “on” was with a 5V signal and “off” was done with a 0V signal. With the correct software inversion and powerboard applying the 12V buffer, this circuit has been updated.

Similar to the analog fault return line, the 5V buffer output to precharge has changed from a BJT to one n-channel MOSFET. The same circuit applies as the powerboard circuit, but precharge does not need to buffer a 12V signal on its own board as it originally only buffered a 5V signal.

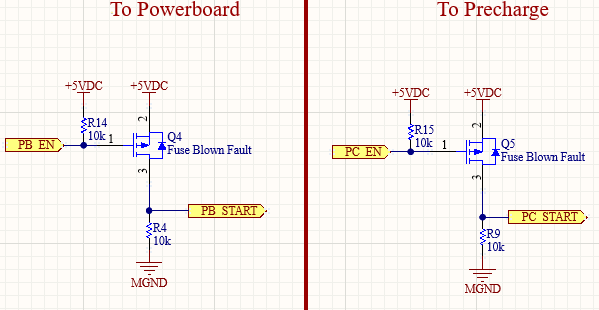


Figure 12 Precharge and powerboard interface

### **PCB Picture**

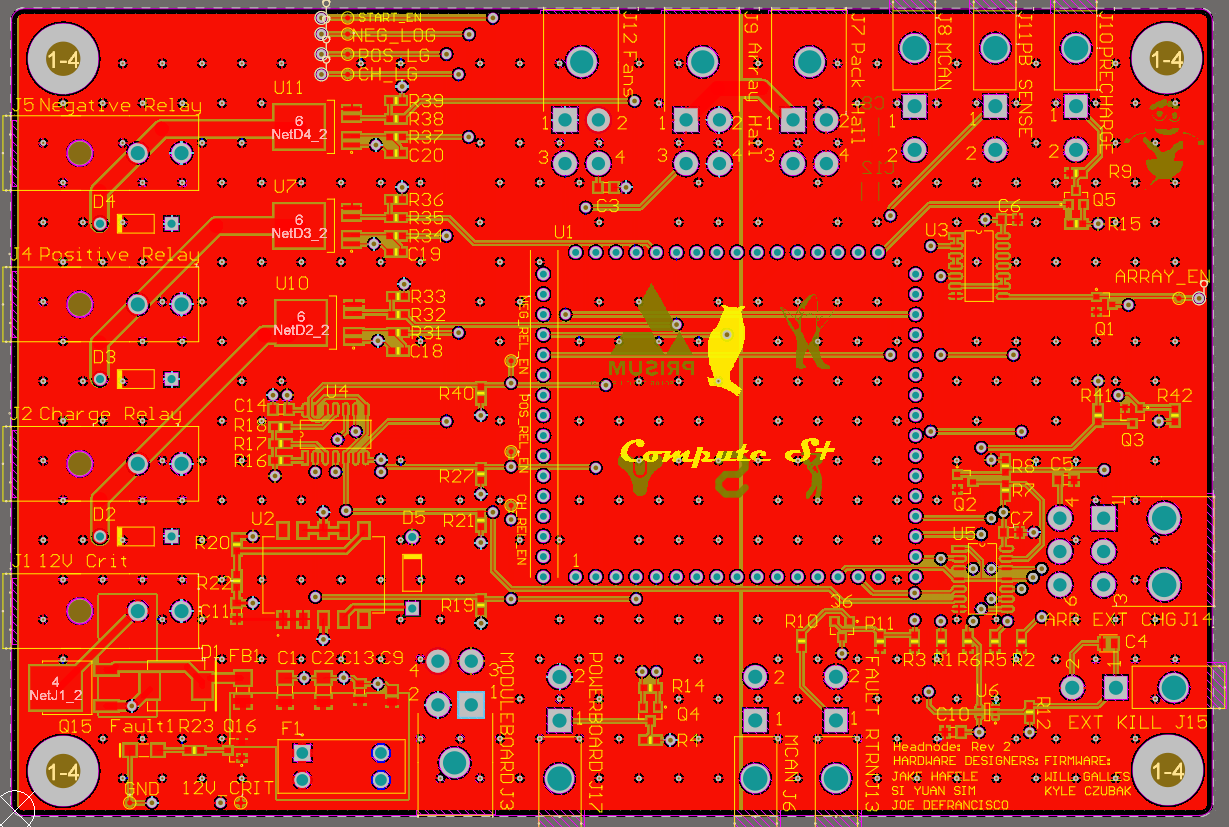


Figure 14 PCB layout of head node

Head node was laid out with the intention to divide the PCB into two parts to accommodate a 12V domain (left) and a 5V digital domain (right). It also uses four layers with the middle two layers being a 5V plane and a solid intact ground plane. The top and bottom layer for the left side (12V domain) is a 12V plane which is stitched together using stitching vias which would allow for maximum current to be shunted to the necessary outputs. This left side basically consists of the switches as well as its supporting logic to turn them on.

The right side on the other hand consists of all the digital logic operating at 5V. This includes the hardware interfacing logic as well as the other circuits operating at 5V. The bottom and top layers are covered by a ground plane which would isolate the noise produced by digital circuits during high speed switching.

# **Proof of Operation**

## **Test Procedure**

1. Test 12V and 5V rails
   1. Connect J1 to a 12V source and measure the test point 12V\_Crit to check if power propagated across the fuse.
   2. Check the right large tab on U8 and ensure that it is outputting 5V.
2. Check turn on logic
   1. Provide 5V to pin 1 of J13 which is the analog fault return line.
   2. Short J15 (external kill) across each other to ground.
   3. Provide 5V to the pin PA13 at the compute using a supply.
   4. Measure pin 6 of U5 (second from bottom left) and ensure it is high at 5V.
   5. Remove each of the above inputs and check pin 6 once again and ensure that it turns low.
3. Check turn on for relays
   1. Keep the above signals high
   2. Check the test points CH\_LG, POS\_LG and NEG\_LG and check if they went high
   3. If they went high and no clicking sounds can be heard from the relays, there is most likely an issue with the buffer.
   4. If they went low instead, there might be an issue with the AND gate.
4. Check output buffers for Powerboard and Precharge
   1. For precharge, give pin PA27 on the compute pin 5V and check pin 1 of J10 and check for 5V.
   2. For powerboard, give pin PB10 on the compute pin 5V and check pin 1 of J17 and check for 5V.
   3. In either case, if both are not giving the expected outputs, ensure that the correct MOSFETs are used with the correct type.

## **Test Results**

The board works as intended accordingly as explained in the project details.

## **Troubleshooting**

1. A common issue found was that the digital logic gates were easily overloaded if too small values of pulldown resistors were used. This would draw out too much current from the AND gates preventing a strong pull to the 5V rails for a high signal.
2. Due to the mix match of transistors used in this circuit, if anything is behaving unexpectedly, it would be significantly easier to isolate the cause to a particular circuit and start unsoldering one transistor after another and testing if the remaining transistor on board works. It is unadvised to reuse transistors.
3. If it is suspected wrong transistors were put on, it is much easier to just put on a new one that it is known that it is of the correct type as it is hard to attempt to figure the type of transistor as well as its chemistry.

## **Future Considerations**

1. Old external charging logic in the interface schematic page could further be removed due to redundancies. All of the external charge logic is now being handled on CAN Bridge (or by the other name, EDNA), and is currently being left as it isn’t taking up too much space.

# **Additional Resources**

## **PrISUm Contacts**

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **ISU Email** | **Personal Email** | **Phone** |
| Jake Hafele | [jmhafele@iastate.edu](mailto:jmhafele@iastate.edu) | [jakehafele@gmail.com](mailto:jakehafele@gmail.com) | 309-696-0228 |
| Si Yuan Sim | [simsy@iastate.edu](mailto:simsy@iastate.edu) | [simsiyuan@gmail.com](mailto:simsiyuan@gmail.com) | 515-2008140 |

# **Appendix**

## **BOM List**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **General Part** | **PCB Label** | **Custom Reference** | **Manufacturer Number** | **Retailer Number** | **Package Size** | **Value** |
| 12V Zener | D1 | Headnode D1 | SMCJ12A | SMCJ12ALFCT-ND |  |  |
| Rectifier Diode | D2, D3, D4, D5 | Headnode D2, D3, D4, D5 | 1N4001-T | 1N4001DICT-ND |  |  |
| Red LED | Fault1 | Headnode Fault1 | HSMH-C150 | 516-1439-1-ND | 1206 |  |
| 10 uF 16V Cap | C1 | Headnode C1 | CL31A106MOHNNNE | 1276-2877-2-ND | 1206 | 10 uF 16V |
| 1 uF 16V Cap | C2 | Headnode C2 | CL31F105ZOCNNNC | 1276-2857-2-ND | 1206 | 1 uF 16V |
| 0.1 uF 50V Cap | C9 | Headnode C9 | 08055C104JAT2A | 478-3352-2-ND | 805 | 0.1 uF 50V |
| 10 nF 100V Cap | C3, C5, C6, C7, C10, C11, C13, C14, C15, C16, C17 | Headnode C3, C5, C6, C7, C10, C11, C13, C14, C15, C16, C17 | CGA3E2X8R2A103K080AD | 445-8825-2-ND | 603 | 10 nF 100V |
| 10 pF 50V Cap | C8, C12 | Headnode C8, C12 | C0805C100G5GACTU | 399-C0805C100G5GAC7800TR-ND | 805 | 10 pF 50V |
| Inverter | U6 | Headnode U6 | SN74AHCT1G04DCKR | 296-4706-1-ND |  |  |
| 3 Channel 3 Input AND | U4, U5 | Headnode U4, U5 | MC14073BDG | MC14073BDGOS-ND |  |  |
| Quad Channel 2 Input NAND | U3 | Headnode U3 | 74AC00SCX | 74AC00SCXCT-ND |  |  |
| PMOS | Q15 | Headnode Q15 | FDD4141 | FDD4141CT-ND |  |  |
| NMOS | Q1, Q2, Q3, Q4, Q5, Q6 | Headnode Q1, Q2, Q3, Q4, Q5, Q6 | MGSF1N03LT1G | MGSF1N03LT1GOSCT-ND |  |  |
| PMOS | Q16 | Headnode Q16 | IRLML6402TRPBF | IRLML6402PbF |  |  |
| High Side Switch | U7, U10, U11 | Headnode U7, U10, U11 | BTF500601TEAAUMA1 | BTF500601TEAAUMA1TR-ND |  |  |
| 1k Res | R10, R12, R33, R36, R39 | Headnode R10, R12, R33, R36, R39 | RC0603FR-071KL | 311-1.00KHRCT-ND | 603 | 1k |
| 10k Res | R1, R2, R3, R4, R5, R6, R7, R8, R9, R11, R12, R14, R15, R16, R17, R18 R19, R21, R27, R31, R32, R34, R35, R37, R38, R40 | Headnode R1, R2, R3, R4, R5, R6, R7, R8, R9, R11, R12, R14, R15, R16, R17, R18 R19, R21, R27, R31, R32, R34, R35, R37, R38, R40 | RC0603FR-0710KL | 311-10.0KHRCT-ND | 603 | 10k |
| Ferrite Bead | FB1 | Headnode FB1 | HI1206N800R-10 | 240-2409-2-ND | 1206 | 80 Ohm |
| 5V Switching Reg | U2 | Headnode U2 | R-78AA5.0-1.0SMD-R | 945-1044-2-ND |  |  |
| 2 Pin Minifit | J6, J8, J10, J11, J13, J15, J17 | Headnode J6, J8, J10, J11, J13, J15, J17 | 39300020 | WM21351-ND |  |  |
| 4 pin Minifit | J3, J7, J9, J12 | Headnode J3, J7, J9, J12 | 39301040 | WM1352-ND |  |  |
| 6 Pin Minifit | J14 | Headnode J14 | 39301060 | WM1352-ND |  |  |
| 2 Pin Megafit | J2, J4, J5 | Headnode J2, J4, J5 | 768250002 | WM11969-ND |  |  |
| Blade Fuse Holder | F1 | Headnode F1 | 3568 | 36-3568-ND |  |  |